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09/410,202	09/30/1999	BRIAN DONOVAN	7134.007	6524
7590	02/09/2005		EXAMINER	
CHERNOFF VILHAUER MCCLUNG & STENZEL 1600 ODS TOWER 601 SW SECOND AVENUE PORTLAND, OR 972043157			ENG, DAVID Y	
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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/410,202
Filing Date: September 30, 1999
Appellant(s): DONOVAN, BRIAN

William O. Geny
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the action of The Board of Patent Appeals and Interferences entered on July 02, 2004. The Supplemental Examiner's Answer is to clarify the factual support of the Examiner's position re claims 4, 2 and 8 as below. The grounds of rejection remain the same.

With respect to the Examiner's motivation statement concerning claim 4 set forth in lines 3-10 of page 7 of the Examiner's Answer, the difference between claim 4 and Madnick is that Figure 4-1 of Madnick shows a process view of an interrupt and task change processing circuit rather than a circuit view (rectangular box format of claim 4) of the interrupt and task change processing circuit. Official Notice is taken by the Examiner that the process shown in Figure 4.1 of Madnick is meant to be executed by a general purpose computer having circuits because that is the sole purpose of a program. In fact, the very fact that the schedulers of Madnick are programs suggests to one of ordinary skill in the art that they are meant to be executed in a general purpose computer. Therefore, it would have been obvious to a person of ordinary skill in the art to execute the Job Scheduler and the Process Scheduler of Madnick by a general purpose computer such that the processes of the two Schedulers can be carried out. The circuits of the general purpose computer which implement the Job Scheduler and the Process Scheduler shown in Figure 4.1 of Madnick are equivalent to the circuits recited in claim 4.

With respect to the Examiner's motivation statement concerning claim 2 set forth in lines 9-11 of page 8 of the Examiner's Answer, Madnick does not show an integrated circuit. Processor fabricated on an IC chip is well known in the art. Official Notice is taken by the Examiner that general purpose computer is commonly built from IC chips because they are basic building blocks of general purpose computer. IC chips are therefore in any general purpose computer.

With respect to the Examiner's motivation statement concerning claim 8 set forth in lines 4-11 of page 9 of the Examiner's Answer, Madnick taught claim combination set forth above. Further, Madnick, in the first paragraph of page 209 and page 212, taught a traffic controller for keeping track of status of all processes. Madnick does not have a trace circuit for recording state information. However, George taught a trace circuit for recording state information when interrupts happened. Attention of the Board is respectfully directed to column 3, et seq. line 19 and column 21 et seq. lines 25. In lines 24-25 of column 3, George further taught that the trace circuit is useful for diagnostic purposes. From the teaching of George, it would have been obvious to a person of ordinary skill in the art to incorporate a trace circuit as taught by George in the traffic controller of Madnick for recording state information for diagnostic purposes.

For the reasons set forth above and in the Examiner's Answer, it is believed that the propriety of the rejections of claims 2, 4-8 and 14-16 remain intact. Accordingly, it is

respectfully requested that the Final Rejection of claims 2, 4-8 and 14-16 be sustained.

Respectfully submitted,



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PRIMARY EXAMINER

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October 15, 2004

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